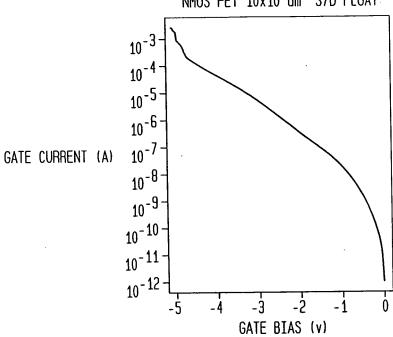
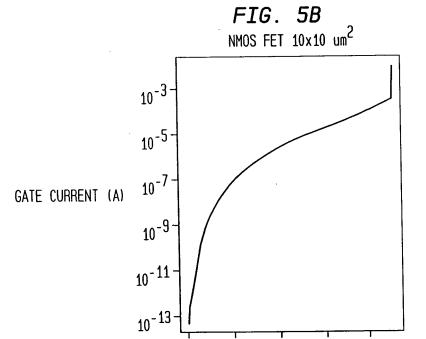


FIG. 5A NMOS FET 10x10 um² S/D FLOAT





GATE BIAS (v)

FIG. 6A GATE OXIDE FUSE

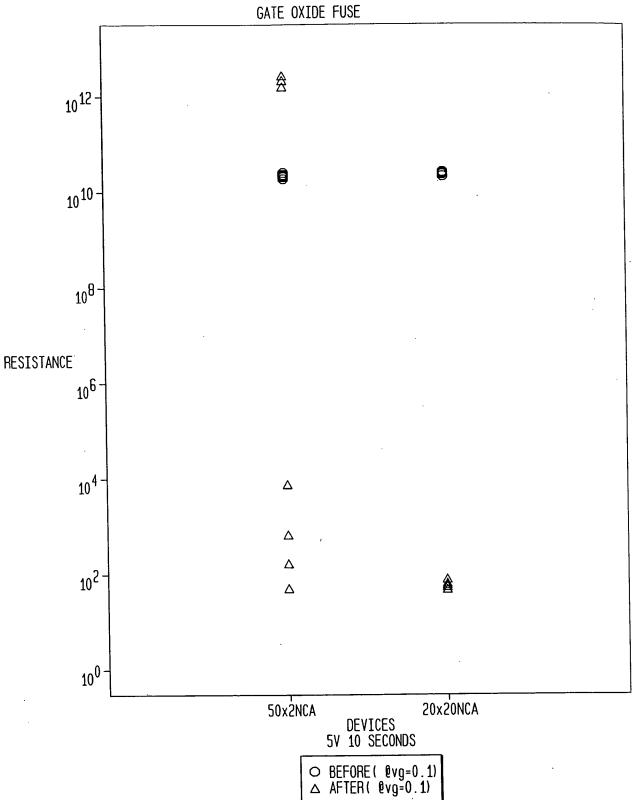


FIG. 6B

